IN THE CLAIMS

1. (Currently Amended) An amplifying circuit, comprising:

an amplifying element with at least an input terminal and an output terminal;

a signal input node, the signal levels of which at least two moments in time are to be amplified by the amplifying element;

at least two connecting lines between the signal input node and the amplifying element, for transferring a signal from the signal input node to the input terminal of the amplifying element;

a memory element on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time;

an input switching element disposed one each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element;

~~at least one output switching element~~ a first output switching element coupled to the output terminal of the amplifying element;

a second output switching element coupled to the output terminal of the amplifying element without connection through the first output switching element;

a first readout bus coupled to the ~~at least one output switching element~~ first output switching element;

a second readout bus coupled to the second output switching element ~~at least one output element~~; and

an output amplifier coupled to the first and second readout buses.

2. (Previously Presented) The amplifying circuit according to claim 1, further comprising a memory element on each of the connecting lines.

3. (Canceled)

4. (Canceled)

5. (Previously Presented) The amplifying circuit according to claim 1, wherein the amplifying element is a transistor of the type of metal oxide semiconductor transistors.

6. (Previously Presented) The amplifying circuit according to claim 1, wherein the amplifying element is an operational transconductance amplifier.

7. (Previously Presented) The amplifying circuit according to claim 1, wherein the memory element is a capacitor.

8. (Currently Amended) An array of amplifying circuits, each amplifying circuit, comprising:

an amplifying element with at least an input terminal and an output terminal;

a signal input node, the signal levels of which at least two moments in time are to be amplified by the amplifying element;

at least two connecting lines between the signal input node and the amplifying element, for transferring a signal from the signal input node to the input terminal of the amplifying element;

a memory element on at least one of the connecting lines, for storing a signal level of the signal input node at a moment in time;

a switching element disposed on each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided

on the connecting line, for consecutively connecting signal levels of the signal input node at different moments in time to the same amplifying element;

a first output switching element coupled to the output terminal of the amplifying element;

a second output switching element coupled to the output terminal of the amplifying element without connection through the first output switching element;

a first readout bus coupled to the first output switching element;

a second readout bus coupled to the second output switching element; and

an output amplifier coupled to the first and second readout buses, wherein the first and second readout buses are coupled to each of the array of amplifying circuits.

9. (Currently Amended) A device for imaging applications, comprising:

a matrix of active pixels arranged in a geometric configuration, each pixel producing an electrical signal indicative of the light intensity of a portion of a scene being imaged by that pixel;

at least one amplifying circuit common to a group of pixels out of the matrix, wherein each amplifying circuit comprises:

an amplifying element with at least an input terminal and an output terminal;

a signal input node being intended to obtain electrical signals from pixels out of the group of pixels to which the amplifying circuit is common, the signal levels of which are to be amplified by the amplifying element;

at least two connecting lines between the signal input node and the amplifying element, for transferring an electrical signal from the signal input node to the input terminal of the amplifying element;

a memory element on at least one of the connecting lines, for storing a signal level of the electrical signal at the signal input node at a moment in time;

a switching element disposed on each connecting line, between the memory element and the input terminal of the amplifying element if a memory element is provided on the connecting line, for consecutively connecting signal levels of the electrical signals at the signal input node at different moments in time to the same amplifying element;

~~at least one output switching element~~ a first output switching element coupled to the output terminal of the amplifying element;

a second output switching element coupled to the output terminal of the amplifying element;

a first readout bus coupled to the ~~at least one output switching element~~ first output switching element;

a second readout bus coupled to the second output switching element without connection through the first output switching element ~~at least one output element~~; and

an output amplifier coupled to the first and second readout buses, wherein the first and second readout buses are coupled to each amplifying circuit.

10. (Previously Presented) The device according to claim 9, wherein the matrix is arranged in columns and rows and wherein the group of pixels is a row of pixels.

11. (Currently Amended) The device according to claim 9, wherein the matrix is arranged in columns and rows and wherein the group of pixels is a column of pixels.

12. (Previously Presented) The device according to claim 9, wherein the first and second readout buses are common to the matrix of active pixels.

Claims 13-16 (Canceled)

17. (Currently Amended) A method for reducing fixed pattern noise of solid state imaging device having a group of active pixels, each pixel comprising a radiation sensitive element and an amplifying circuit, the method comprising:

reading out the signal of a pixel brought in a first state and storing the corresponding voltage level in a first memory element;

reading out the signal of the pixel brought in a second state, which is different from the first state, and storing the corresponding voltage level in a second memory element;

transferring the signal of the first memory element to an amplifying element, amplifying ~~it and~~ the signal of the first memory element, and transferring ~~it~~ the amplified signal of the first memory element to a first readout bus;

transferring the signal of the second memory element to the same amplifying element, amplifying ~~it and~~ the signal of the first memory element, and transferring the amplified signal of the second memory element to a second readout bus in parallel with the transfer to the amplified signal of the first memory element to the first readout bus; and

repeating these steps for at least part of the pixels of the imaging device.

18. (Canceled)

19. (Previously Presented) The method according to claim 17, further comprising calculating a differential output signal by taking the difference between potential values on the first and second readout buses.

20. (Previously Presented) The method according to claim 17, wherein the first state and the second state correspond to different amounts of radiation collected on the radiation sensitive element in the pixel.

21. (Previously Presented) The method according to claim 20, wherein the first state or the second state corresponds to an amount of radiation or light collected on the radiation sensitive element in the pixel.

22. (Previously Presented) The method according to claim 20, wherein the second state or the first state corresponds to a non-irradiated or non-illuminated or dark or reset state or the first state corresponds to a non-irradiated or non-illuminated or dark or reset state of the pixel.

23. (Previously Presented) The method according to claim 17, wherein the pixel is read out in additional states and its corresponding voltage level is being stored on additional memory elements.

24. (Previously Presented) The method according to claim 17, wherein the signal of the first memory element is transferred to the first output line common for the group, and concurrently, the signal of the second memory element of another amplifier is transferred to the second output line common for said group.

25. (Canceled)

26. (Canceled)

27. (Previously Presented) The amplifying circuit according to claim 1, wherein the first readout bus is a signal bus and the second readout bus is a reset bus.

28. (Previously Presented) The amplifying circuit according to claim 27, wherein the output amplifier has a positive input and a negative input and wherein the signal bus is coupled to the positive input and the reset bus is coupled to the negative input.

29. (Previously Presented) The amplifying circuit according to claim 1, wherein a differential signal on the first and second readout buses is proportional to the signal levels of the signal input node.

30. (Canceled)